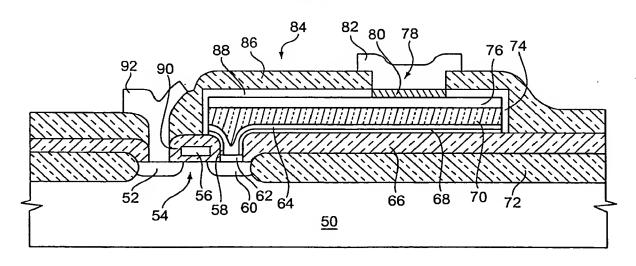
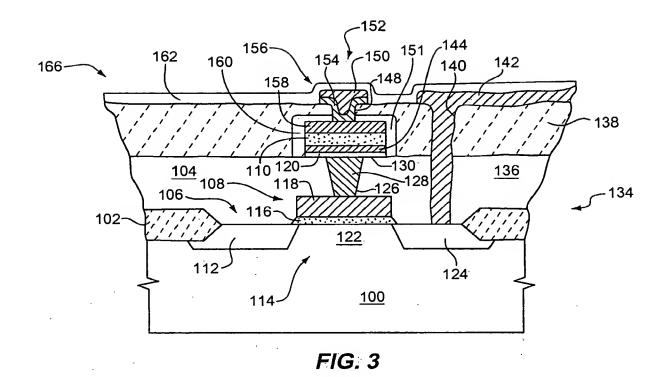


FIG. 2





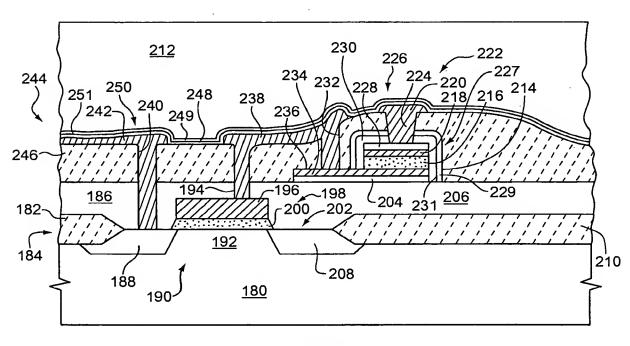


FIG. 4

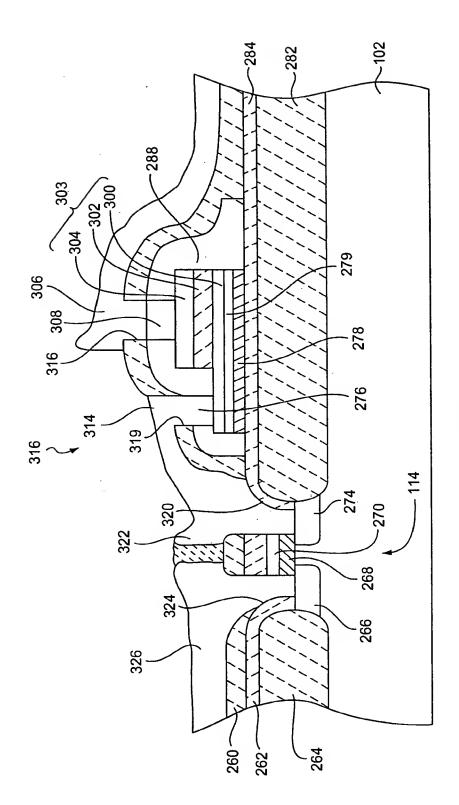


FIG. 5

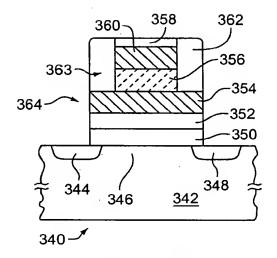


FIG. 6

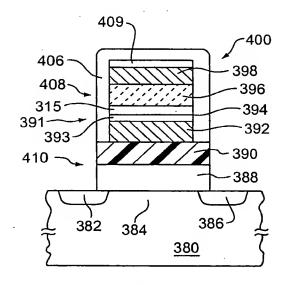
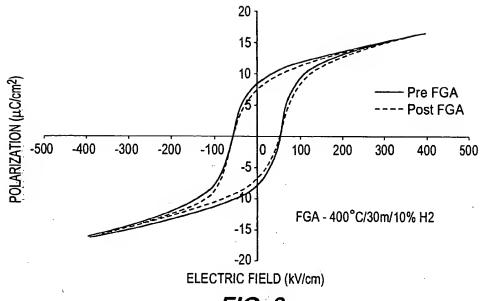


FIG. 7





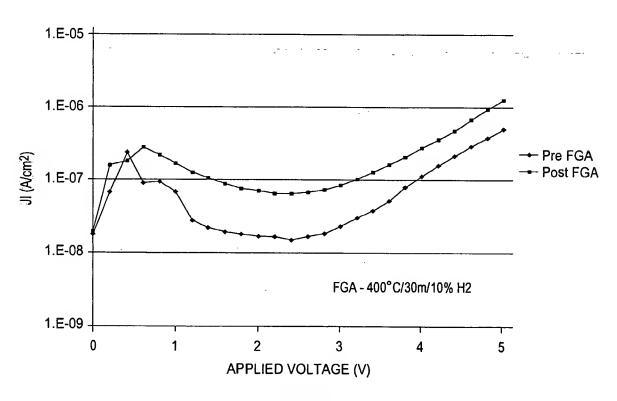


FIG. 9

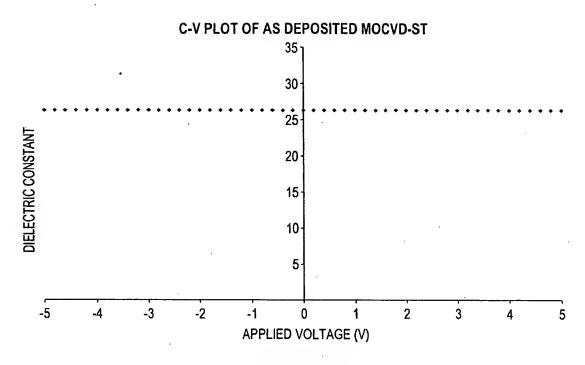


FIG. 10

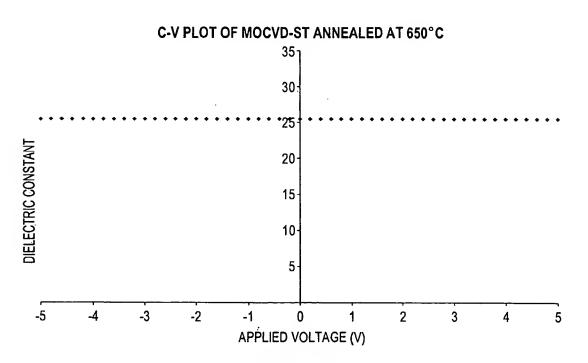


FIG. 11

FIG. 12 -500 PROVIDE SUBSTRATE DEPOSIT GATE INSULATOR ~502 DEPOSIT GATE ELECTRODE **- 508 USE MOCVD TO** APPLY FIRST INSULATIVE -510 -542 PATTERN FET HYDROGEN BARRIER **DEPOSIT ILD** -512 PATTERN INSULATIVE -544 **BARRIER** FORM VIA AND PLUG -516 APPLY ILD AND **-556 FORM VIAS DEPOSIT CONDUCTIVE** - 520 HYDROGEN BARRIER FORM CONDUCTIVE -558 HYDROGEN BARRIER **DEPOSIT BOTTOM** - 524 **ELECTRODE** APPLY METALIZATION **-560** - 528 **DEPOSIT OXIDE CONDUCT FGA** -566 TREAT OXIDE 530 **DEPOSIT SECOND INSULATIVE** -570 HYDROGEN BARRIER **DEPOSIT TOP** -532 **ELECTRODE COMPLETE IC** -574 PATTERN AND TREAT -538 **CAPACITOR**

FIG. 13

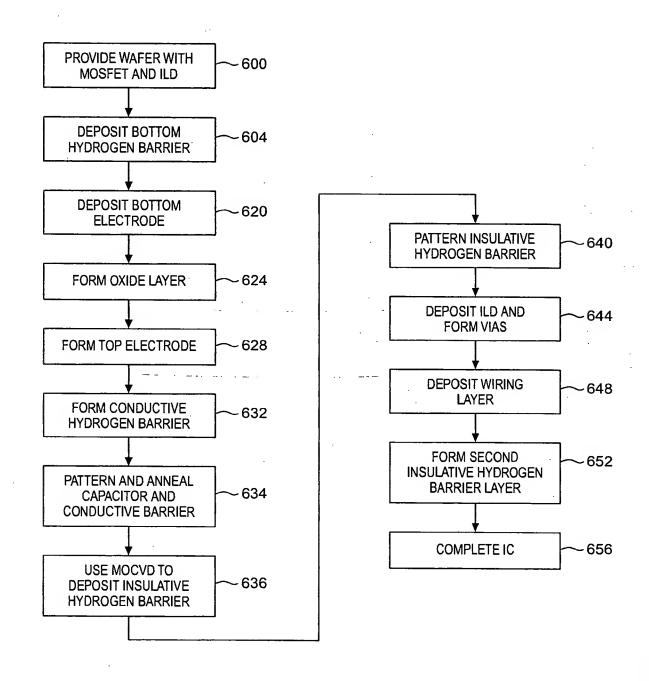


FIG. 14

